

Master 2 Research Internship and Ph.D. Proposal

Laboratory: Centre de Nanosciences et de Nanotechnologies (C2N)
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Nanodevices for Energy-Efficient AI: Overcoming Imperfections through Learning

You will combine experiments on real memory chips with learning algorithms to make energy-efficient AI more reliable. This primarily experimental project is particularly suited to students in physics, nanoelectronics or electrical engineering who enjoy laboratory work, mathematics and programming. You will measure devices, write code to control experiments, and develop algorithms that help neural networks operate with imperfect hardware. **The necessary background in deep learning can be acquired during the project.**

Reducing the energy consumption of AI requires reinventing the electronics that run it. A neural network processes information using adjustable numerical parameters called weights. Storing these weights in nanoscale memory devices allows computations to take place in or close to memory, reducing the energy spent moving data between separate components. This approach can be remarkably efficient: our group has for example demonstrated the Bayesian machine [1] and a memristor-based AI circuit powered by a miniature solar cell [2].

The difficulty is that physical devices do not always store the weights we want. Memristors, which encode information through their electrical resistance, can be difficult to program precisely, and their stored values may change over time. Differences between devices introduce further errors. As a result, a neural network that performs well in software can lose accuracy when transferred to a chip.

Our goal is to use a small amount of learning directly on the chip to compensate for these imperfections. Starting from a network trained in software, you will investigate how a limited number of adjustments can recover accuracy after programming and maintain it as the hardware evolves. The central challenge is to achieve this with sufficiently few updates to preserve the hardware's energy advantage and limit device wear. You will build on learning methods developed in our group for physical memory devices, including approaches that reuse the operations already needed to make predictions [3,4].

The experiments will explore memristor arrays and ferroelectric random-access memories (FeRAM), which store information through electrical polarization. Our recent work in Nature Electronics demonstrated a hybrid ferroelectric-memristor memory that combines complementary devices for learning and for running trained networks [5]. Other results also show how algorithms that account for device physics can enable experimental neural networks to operate with variable and imperfect components [6,7,8]. These results provide a foundation for developing and testing new approaches on real hardware.

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During the Master's internship, you will focus on one memory technology and a small neural-network task, starting from existing experimental platforms and research code. You will characterize programming errors or changes in stored weights, measure their effect on the network's accuracy, and test a learning rule that adjusts the physical devices. A concrete objective will be to demonstrate improved accuracy after a limited number of updates and assess the associated programming effort and energy cost. Electrical measurements, data analysis and algorithm development will be closely connected throughout the work.

During the PhD, you will develop and experimentally demonstrate learning methods that help memristor- and FeRAM-based AI systems maintain their performance over time. You will investigate which parts of a network need adjustment, when learning should be triggered, and how few examples and programming operations are needed. Measurements of device behavior will guide the algorithms, while experiments will assess the trade-offs between model performance, energy consumption and device wear. The experimental demonstrations could extend to compact generative AI models, providing a demanding test of these methods.

You will join the interdisciplinary INTEGNANO group at C2N, Université Paris-Saclay/CNRS, working at the intersection of device physics, electronics and artificial intelligence. The project will involve collaboration

with Elisa Vianello's group at CEA-Leti. You will develop expertise in electrical characterization, experimental automation and modern machine learning/AI, with opportunities to shape the research around your strengths and interests. For more technical details on the project, contact us!

Selected references

- [1] K.-E. Harabi, ..., D. Querlioz, "A memristor-based Bayesian machine", **Nature Electronics** 6, 52–63 (2023).
- [2] F. Jebali, ..., D. Querlioz, J.-M. Portal, "Powering AI at the edge: A robust, memristor-based binarized neural network with near-memory computing and miniaturized solar cell", **Nature Communications** 15, 741 (2024).
- [3] T. Dalgaty, ..., D. Querlioz, E. Vianello, "In situ learning using intrinsic memristor variability via Markov chain Monte Carlo sampling", **Nature Electronics** 4, 151–161 (2021).
- [4] A. Renaudineau, ..., D. Querlioz, "Forward-only learning in memristor arrays with month-scale stability", arXiv:2601.09903 (2026), preprint.
- [5] M. Martemucci, ..., D. Querlioz, E. Vianello, "A ferroelectric–memristor memory for both training and inference", **Nature Electronics** 8, 921–933 (2025).
- [6] D. Bonnet, ..., D. Querlioz, E. Vianello, "Bringing uncertainty quantification to the extreme-edge with memristor-based Bayesian neural networks", **Nature Communications** 14, 7530 (2023).
- [7] D. Bonnet, ..., D. Querlioz, "Bayesian continual learning and forgetting in neural networks", **Nature Communications** 16, 9614 (2025).
- [8] D. Querlioz and E. Vianello, "Bayesian electronics for trustworthy artificial intelligence", **Nature Reviews Electrical Engineering** 2, 846–855 (2025).