Centre de Nanosciences et de Nanotechnologies

Soutenance de thèse

Vendredi 22 février

14h 30
Salle Amphithéâtre du Centre d'intégration Nano-INNOV du Bât 862

Gefei WANG

"Design and Development of new logic circuits based on spin field-effect transistor"

Jury members :

Cristell MANEUX	Professeur	Bordeaux University	Rapporteur
Lionel TORRES	Professeur	University of Montpellier	Rapporteur
Weisheng ZHAO	Professeur	Beihang University	Examinateur
Jacques-Olivier KLEIN	Professeur	Université Paris Saclay	Directeur de thèse
Dafiné RAVELOSONA	Directeur de Recherche	Université Paris Saclay	Examinateur
Sébastien LE BEUX	Associate Professor	École Centrale de Lyon	Examinateur

Abstract :

The development of Complementary Metal Oxide Semiconductor (CMOS) technology drives the revolution of the integrate circuits (IC) production. Each new CMOS technology generation is aimed at the fast and low-power operation which mostly benefits from the scaling with its dimensions. However, the scaling will be influenced by some fundamental physical limits of device switching since the CMOS technology steps into sub-10 nm generation. Researchers want to find other ways for addressing the physical limitation problem. Spintronics is one of the most promising fields for the concept of non-charge-based new IC applications. The spin-transfer torque magnetic random access memory (STT-MRAM) is one of the successful spintronics-based memory devices which is coming into the volume production stage. The related spin-based logic devices still need to be investigated. Our research is on the field of the spin field effect transistors (spin-FET), one of the fundamental spin-based logic devices. The main mechanism for realizing a spin-FET is controlling the spin of the electrons which can achieve the objective of power reduction. Moreover, as spin-based devices, the spin-FET can easily combine with spin-based storage elements such as magnetic tunnel junction (MTJ) to construct the "non-volatile logic" architecture with high-speed and low-power performance. Our focus in this thesis is to develop the compact model for spin-FET and to explore its application on logic design and non-volatile logic simulation.
Firstly, we proposed the non-local geometry model for spin-FET to describe the behaviors of the electrons such as spin injection and detection, the spin angle phase shift induced by spin-orbit interaction. We programmed the non-local spin-FET model using Verilog-A language and validated it by comparing the simulation with the experimental result. In order to develop an electrical model for circuit design and simulation, we proposed the local geometry model for spin-FET based on the non-local spin-FET model. The investigated local spin-FET model can be used for logic design and transient simulation on the circuit design tool.
Secondly, we proposed the multi-gate spin-FET model by improving the aforementioned model. In order to enhance the performance of the spin-FET, we cascaded the channel using a shared spin injection/detection structure. By designing different channel length, the multi-gate spin-FET can act as different logic gates. The performance of these logic gates is analyzed comparing with the conventional CMOS logic. Using the multi-gate spin-FET-based logic gates, we designed and simulated a number of the Boolean logic block. The logic block is demonstrated by the transient simulation result using the multi-gate spin-FET model.
Finally, combing the spin-FET model and multi-gate spin-FET model with the storage element MTJ model, the "non-volatile logic" gates are proposed. Since the only pure spin signal can reach to the detection side of the spin-FET, the MTJ receives pure spin current for the spin transfer. In this case, the switching of the MTJ can be more effective compared with the conventional MTJ/CMOS structure. The performance comparison between hybrid MTJ/spin-FET structure and hybrid MTJ/CMOS structure are demonstrated by delay and critical current calculation which are derived from Landau-Lifshitz-Gilbert (LLG) equation. The transient simulation verifies the function of the MTJ/spin-FET based non-volatile logic.

UMR9001 CNRS-UPSUD
10 Boulevard Thomas Gobert
91120 Palaiseau