Soutenance de thèse

Lundi 13 février
14h00 - Amphithéâtre

Semi-empirical and ab-initio simulation of quantum transport in nanoscale devices

Adel M'FOUKH

Jury members :

Fabienne Michelini, Professeure des universités, Aix-Marseille Université, Rapporteuse
Mathieu Luisier, Professeur, ETH Zurich, Rapporteur
Frédéric Aniel, Professeur des universités, Université Paris Saclay, Examinateur
Demetrio Logoteta, Chercheur, Université de Rome La Sapienza, Examinateur
Marco Pala, Directeur de thèse Directeur de recherche, CNRS, Université Paris Saclay,
Philippe Dollfus, Directeur de recherche, CNRS, Université Paris Saclay, Co-encadrant
David Esseni, Professeur, Université d'Udine, Invité

Abstract :

The aggressive shrinking of transistor sizes by the microelectronics industry has reached the nanoscale. The performance of components at this scale is strongly impacted by quantum phenomena (tunnelling, interference, etc.) but also the electrostatic control becomes more delicate. In order to improve the performance of components, it is essential to take these phenomena into account and to explore alternatives to the silicon-based MOSFET that is the current reference. This task can be supported by a rigorous theoretical approach for electronic material properties and thus simulate the performance of the devices.

In this thesis, we propose to extend the state of the art in this field by developing an electronic transport model based on the non-equilibrium Green's function formal-ism. The particularity of our approach is the use of pseudopotential Hamiltonians based on plane waves obtained by either a semi-empirical or an ab-initio approach. This type of Hamiltonian allows us to obtain an atomistic description of the material and thus to have an accurate description at the microscopic scale.

In a first part, we developed the empirical pseudopotential Hamiltonian model to study III/V material heterostructures (InAs/GaSb) with a non-abrupt inter-face. This method has been applied to the study of tunnelling based devices, Esaki diode and tunnel FET. The results show a degradation of the current when the transition region is long. A comparison with an experimental study also showed the accuracy of our simulations.

In the following parts of the thesis, the focus is on the Hamiltonians obtained from ab-initio calculations. We started with the development of a model to study the Hamiltonians of heterostructure by investigating two approaches, one based on the Hamiltonian of isolated material and the second based on the Hamiltonian of a supercell of the heterostructure. The models were applied to two components, a MOSFET composed of monolayer and bilayer $PtSe_2$ and a tunnel FET composed of monolayer $PdSe_2$ and monolayer SnS_2. This highlighted that the study of the interface between two distinct materials requires the use of sophisticated approaches to describe the coupling between the materials. To improve the model, we then included electron-phonon interactions in our simulations. We first used deformation potentials, fully derived from ab-initio calculations, to describe the coupling with phonons under the self-consistent Born approximation. This model has been applied to the study of a tunnel FET made with the heterostructure of a monolayer $HfSe_2$ and a monolayer SnS_2. Two different architectures were studied, one with a vertical stacking of the 2D materials and a lateral heterostructure. The results show that phonons play an important role for the transmission properties by introducing an increase in current through inter-valley transmission. Finally, the vertical heterostructure emerges as the most promising candidate with a sub-threshold slope of 40 mV/dec for an ON state current of 580 mA/µm at V_{DD}= 0.35 V.

In the last part of the thesis, a more rigorous description of the electron-phonon coupling for transport was proposed. We have developed a model using ab-initio calculations of the electron-phonon matrix elements and phonon frequencies. This model was compared to the literature and to the deformation potential method by studying the monolayer MoS_2 with mobility calculations. Finally, the study of a CMOS was carried out using an n-type (with monolayer MoS_2) and a p-type (with monolayer WSe_2) MOSFET. Despite the phonon scattering, the devices satisfy the predictions for the next generation of transistors.

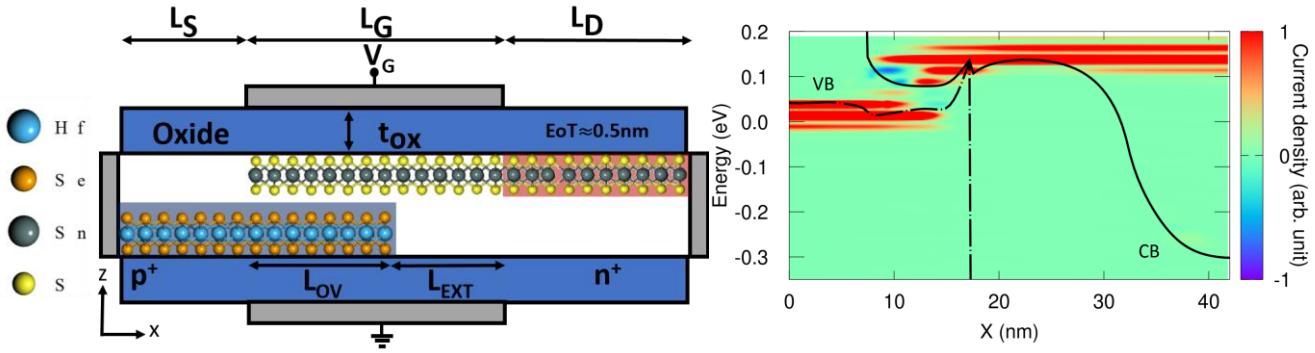

Figure 1 (left) $HfSe_2/SnS_2$ van der Waals tunnel FET sketch. (right) Current spectrum and conduction band (solid line) and valence band (dashed line) profiles along the device in OFF state.

UMR9001
10 boulevard Thomas Gobert
91120 Palaiseau